WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a first device formed on the insulating layer, comprising:

a first fin formed on the insulating layer and having a first fin aspect ratio; and

a second device formed on the insulating layer, comprising:

a second fin formed on the insulating layer and having a second fin aspect ratio different from the first fin aspect ratio.

2. The semiconductor device of claim 1, wherein the first device is an NMOS device and the second device is a PMOS device.

3. The semiconductor device of claim 1, wherein the first device and the second device are included in a single circuit element.

4. The semiconductor device of claim 1, wherein a first carrier mobility in the first fin of the first device is different from a second carrier mobility in the second fin of the second device.

5. The semiconductor device of claim 1, wherein the first device further includes:

a first gate dielectric formed on at least three surfaces of the first fin, and

a first gate material formed on the at least three surfaces of the first fin; and

wherein the second device further includes:

a second gate dielectric formed on at least three surfaces of the second fin, and

a second gate material formed on the at least three surfaces of the second fin.

6. The semiconductor device of claim 5, wherein the first gate dielectric and the first gate material are formed on four surfaces of the first fin.

7. The semiconductor device of claim 6, wherein the second gate dielectric and the second gate material are formed on four surfaces of the second fin.

8. A semiconductor device, comprising:

an insulating layer;

a first device formed on the insulating layer, comprising:

a first fin formed on the insulating layer and having a first height and a first width,

a first dielectric layer formed on at least three sides of the first fin, and

a first gate adjacent the first dielectric layer; and

a second device formed on the insulating layer, comprising:

a second fin formed on the insulating layer and having a second height and a second width,

a second dielectric layer formed on at least three sides of the second fin, and

a second gate adjacent the second dielectric layer,

wherein a first ratio of the first height and first width is different from a second ratio of the second height and second width.

9. The semiconductor device of claim 8, wherein the first device is an NMOS device and the second device is a PMOS device.

10. The semiconductor device of claim 8, wherein the first device and the second device are included in a single circuit element.

11. The semiconductor device of claim 8, wherein a first carrier mobility in the first fin of the first device is about equal to a second carrier mobility in the second fin of the second device.

12. The semiconductor device of claim 8, wherein the first device is a π-gate FinFET, a u-gate FinFET, or a round-gate FinFET.

13. The semiconductor device of claim 12, wherein the second device is a π-gate FinFET, a u-gate FinFET, or a round-gate FinFET.

14. The semiconductor device of claim 8, further comprising:

a third device formed on the insulating layer, comprising:

a third fin formed on the insulating layer and having a third height and a third width,

a third dielectric layer formed on at least three sides of the third fin, and

a third gate adjacent the third dielectric layer,

wherein a third ratio of the third height and third width is different from the first ratio and the second ratio.

15. A semiconductor device, comprising:

an insulating layer;

an N-type device formed on the insulating layer, comprising:

a first fin formed on the insulating layer and having a first height and a first width; and

a P-type device formed on the insulating layer, comprising:

a second fin formed on the insulating layer and having a second height and a second width,

wherein the second width is a predetermined multiple of the first width, and

wherein the first height and the second height are configured so that a carrier mobility of the N-type device approximately equals a carrier mobility of the P-type device.

16. The semiconductor device of claim 15, wherein the predetermined multiple is about 2.

17. The semiconductor device of claim 15, wherein the predetermined multiple is about 1.5.

18. The semiconductor device of claim 15, wherein both the N-type device and the P-type device are π-gate FinFETs, u-gate FinFETs, or round-gate FinFETs.